IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device comprising:

a first main electrode;

a second main electrode;

a semiconductor base region of a first conductivity type;

a gate electrode provided in a trench through an insulating film, the trench being formed to penetrate the semiconductor base region; and

a first semiconductor region of a second conductivity type provided under the semiconductor base region, a second semiconductor region of a first conductivity type provided under the first semiconductor region, a third semiconductor region of a second conductivity type provided under the second semiconductor region, and a fourth semiconductor region of a second conductivity type provided on the semiconductor base region,

the first main electrode being provided on the fourth semiconductor region and the second main electrode being provided under the third semiconductor region,

a flow of a current between the first and second main electrodes when a voltage of a predetermined direction is applied between these electrodes being controllable in accordance with a voltage applied to the gate electrode, and

a depleted region extending from a junction between the first and the second semiconductor regions reaching the trench,

wherein a bottom of the trench is provided within the second semiconductor region.

Claim 2 (Original): The semiconductor device according to claim 1, wherein a forward voltage is applied to a p-n junction formed between the first and second semiconductor regions when the voltage of the predetermined direction is applied between the first and second main electrodes.

Claim 3 (Previously Presented): The semiconductor device according to claim 1, wherein the second semiconductor region is in contact with the trench.

Claim 4 (Canceled).

Claim 5 (Original): The semiconductor device according to claim 1, wherein a plurality of the first semiconductor regions and a plurality of the second semiconductor regions are laminated alternately under the semiconductor base region.

Claim 6 (Previously Presented): The semiconductor device according to claim 1, wherein the second semiconductor region is provided apart from the trench.

Claim 7 (Previously Presented): The semiconductor device according to claim 1, wherein a plurality of the first semiconductor region and the second semiconductor region are arranged alternately on a plane which is substantially perpendicular to a depth direction of the trench.

Claims 8-11 (Canceled).

Claim 12 (Original): A semiconductor device comprising:

a first semiconductor region of a second conductivity type;

a second semiconductor region of a first conductivity type provided on the first semiconductor region,

a third semiconductor region of a second conductivity type provided on the second semiconductor region,

a fourth semiconductor region of a first conductivity type provided on the third semiconductor region,

a fifth semiconductor region of a second conductivity type provided on the fourth semiconductor region,

a trench penetrating at least the third through fifth semiconductor regions, a bottom of the trench being provided between an upper surface and a lower surface of the second semiconductor region;

a sixth semiconductor region of a second conductivity type provided in contact with the bottom of the trench; and

a gate electrode provided in the trench through an insulating film.

Claim 13 (Original): The semiconductor device according to claim 12, wherein the sixth semiconductor region is substantially depleted by a junction with the second semiconductor region.

Claim 14 (Original): The semiconductor device according to claim 12, wherein the second and the third semiconductor regions are substantially depleted.

Claim 15 (Original): The semiconductor device according to claim 12, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than $3 \times 10^{16}/cm^3$.

Claims 16-19 (Canceled).

Claim 20 (Previously Presented): A semiconductor device comprising:

a first semiconductor region of a second conductivity type;

a semiconductor layer provided on the first semiconductor region and having a plurality of second semiconductor regions of a first conductivity type and a plurality of third semiconductor regions of a second conductivity type, the second and the third semiconductor regions being arranged alternately;

a fourth semiconductor region of a first conductivity type provided on the semiconductor layer,

a fifth semiconductor region of a second conductivity type provided on the fourth ssemiconductor region,

a trench penetrating at least the fourth and the fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and

a gate electrode provided in the trench through an insulating film,

wherein carrier concentrations of the second and the third semiconductor regions are equal to or less than $5 \times 10^{15}/cm^3$, and

the trench is in contact with the second semiconductor region and the third semiconductor region.

Claim 21 (Previously Presented): The semiconductor device according to claim 1, wherein the second semiconductor region is in contact with a side of the trench, but is not in contact with a bottom of the trench, and a semiconductor region of a first conductivity type is provided instead.

Claim 22 (Previously Presented): A semiconductor device comprising:

a first semiconductor region of a second conductivity type;

a semiconductor layer provided on the first semiconductor region and having a plurality of second semiconductor regions of a first conductivity type and a plurality of third semiconductor regions of a second conductivity type, the second and the third semiconductor regions being arranged alternately along with two diagonal directions on the first semiconductor region;

a fourth semiconductor region of a first conductivity type provided on the semiconductor layer,

a fifth semiconductor region of a second conductivity type provided on the fourth semiconductor region,

a trench penetrating at least the fourth and the fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and

a gate electrode provided in the trench through an insulating film,

the trench being in contact with the second semiconductor region and the third semiconductor region.

Claim 23 (Previously Presented): The semiconductor device according to claim 22, wherein the second and the third semiconductor regions are substantially depleted.

Claim 24 (Previously Presented): The semiconductor device according to claim 20, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than 3 X $10^{17}/cm^3$.

Claim 25 (Previously Presented): The semiconductor device according to claim 20, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than 3 X $10^{16}/cm^3$.